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EXAMINER
VU, TRISHA U

ART UNIT	PAPER NUMBER
2189	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/738,913	Applicant(s) KOSARAJU, CHAKRAVARTHY	
	Examiner Trisha U. Vu	Art Unit 2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *27 February 2003* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-31 are presented for examination.

Claim Objections

2. Claim 31 is objected to because of the following informalities: missing period at the end of the claim: "the device" should be changed to "the device.". Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 6 and 7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 6 and 7 recite the limitation "the group" in line 1. There is insufficient antecedent basis for this limitation in the claims.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an

international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-7, 13-18, 22, 24-31 are rejected under 35 U.S.C. 102(e) as being anticipated by Arimilli et al. (6,535,939) (hereinafter Arimilli).

As to claim 1, Arimilli teaches an apparatus, comprising: a routing agent (bus allocation unit and/or switch 401) to change one or more communication pathways in a processor without changing a physical component layout in the processor (col. 6 lines 58-67, col. 7 lines 1-10, col. 9 lines 31-46, and col. 10 lines 33-46).

As to claim 2, Arimilli further teaches the routing agent comprises a first component and a second component, the first component (part of the allocation unit) to determine a bandwidth between the device and the processor (monitoring the bus usage on the system) (col. 10, lines 63-67), the second component (part of the allocation unit) to provide a control signal to one or more signal pathway switching devices, the control signal to be based upon the bandwidth determination of the first component (the switch system allocates the available configurable buses based on the change in workload and the priority of the components) (note col. 11, lines 1-11 and also col. 7, lines 1-10 wherein a mode bit may be used to tell the processor how the ports are configured).

As to claim 3, Arimilli further teaches a point-to-point bus, the processor communicates to a device through the point-to-point bus (Fig. 1B and col. 2, lines 56-65).

As to claim 4, Arimilli further teaches the routing agent is internal to the processor (col. 10, lines 42-46 and Fig. 2B).

As to claim 5, Arimilli further teaches the routing agent is external to the processor (col. 10, lines 40-42).

As to claim 6, Arimilli further teaches the device is selected from a group consisting of an input-output component, a bridge, a chipset, a memory, or a second processor (memory, SMPs, or other component) (col. 4, lines 3-12).

As to claim 7, Arimilli further teaches the control signal is selected from a group consisting of an enable signal, a disable signal, an increase clock speed signal, or a set default clock speed signal (note col. 7 lines 1-34 and col. 9 lines 1-30 wherein mode bit may be used to tell the processor how the ports are configured).

As to claim 13, Arimilli teaches a method comprising: sending a control signal to one or more components within a processor having a flexible architecture (col. 11 lines 1-11, col. 7 lines 1-34); and changing one or more communication pathways in the processor without changing a physical component layout in the processor (col. 6 lines 58-67, and col. 10, lines 33-46).

As to claim 14, Arimilli further teaches communicating between the processor and a device through at least one point-to-point bus (Fig. 1B and col. 2, lines 56-65).

As to claim 15, Arimilli further teaches changing a setting in a configuration register (register(s) that hold the setting of the buses) to direct a routing agent to send the control signal to one or more communication pathway switching devices located in the processor (col. 7, lines 2-10, lines 56-64, and col. 8, lines 25-28).

As to claim 16, Arimilli teaches a method comprising: changing a bandwidth between a processor and a device exterior to the processor without changing a physical component layout in the processor (col. 11, lines 1-11).

As to claim 17, Arimilli further teaches communicating between the processor and the device through at least one point-to-point bus (Fig. 1B and col. 2, lines 56-65).

As to claim 18, Arimilli further teaches changing the bandwidth comprises altering a number of ports linked between the processor and the device (col. 9, lines 31-46).

As to claim 22, Arimilli teaches a system, comprising: a processor having a flexible architecture; and a routing agent (bus allocation unit and/or switch 401) to control the one or more communication pathways in the processor (col. 6 lines 58-67, col. 7 lines 1-10, col. 9 lines 31-46, and col. 10 lines 33-46).

As to claim 24, Arimilli further teaches a point-to-point bus, the processor communicates to a device through the point-to-point bus (Fig. 1B and col. 2, lines 56-65).

As to claim 25, Arimilli further teaches the system is selected from a group consisting of a work station, or a server (connection to network) (col. 5, lines 12-26 and col. 11, lines 25-52).

As to claim 26, Arimilli teaches an apparatus, comprising: a means for changing the bandwidth between a processor and a device exterior to the processor without changing a physical component layer in the processor (col. 6 lines 58-67, col. 7 lines 1-10, col. 9 lines 31-46, and col. 10 lines 33-46).

As to claim 27, Arimilli further teaches a means for communicating between the processor and the device through at least one point-to-point bus (Fig. 1B and col. 2, lines 56-65).

As to claim 28, Arimilli further teaches changing the bandwidth comprises altering a number of ports linked between the processor and the device (col. 9, lines 31-46).

As to claim 29, Arimilli teaches an apparatus, comprising: a routing agent (bus allocation unit and/or switch 401) to change the bandwidth between a processor and a device exterior to the processor without changing a physical component layer in the processor (col. 6 lines 58-67, col. 7 lines 1-10, col. 9 lines 31-46, and col. 10 lines 33-46).

As to claim 30, Arimilli further teaches the processor uses a point-to-point bus to communicate with the device (Fig. 1B).

As to claim 31, Arimilli further teaches the routing agent further comprises a configuration register (register(s) that hold the setting of the buses) to alter a number of ports linked between the processor and the device (col. 7, lines 2-10, lines 56-64, and col. 8, lines 25-28).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8-12 and 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (6,535,939) (hereinafter Arimilli) as applied to claims 1 and 22 above, and further in view of Walker (6,321,269).

As to claim 8, Arimilli further teaches the processor comprises an interface for connection to other devices (Fig. 1B). However, Arimilli does not explicitly disclose the processor comprises a protocol layer; an information transfer layer to electronically transfer information on a physical medium between the protocol layer and the device; and a buffer layer to buffer an electronic transfer of information between the protocol layer and the information transfer layer. Walker teaches an information transfer layer (physical layer); a buffer layer (link layer); and a protocol layer (other upper layer(s) of the client/server to further process the data); wherein the information transfer layer is to electronically transfer information on a physical medium between the protocol layer and a device; the buffer layer is to buffer an electronic transfer of information between the protocol layer and the information transfer layer (Fig. 2 and col. 3, lines 49-67, and col. 4, lines 1-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include an information transfer layer, a buffer layer, and a protocol layer as taught by Walker in the system of Arimilli to expand communication to a network.

As to claim 9, Arimilli as modified above further teaches the one or more communication pathways may be changed by altering a signal path that a signal travels in the information transfer layer (col. 6 lines 58-67, col. 7 lines 1-10, and col. 10, lines 33-46).

As to claim 10, Arimilli as modified above further teaches the one or more communication pathways may be changed by altering a signal path that a signal travels in the buffer layer (col. 6 lines 58-67, col. 7 lines 1-10, and col. 10, lines 33-46).

As to claim 11, Arimilli as modified above further teaches the buffer layer consists of at least one communication pathway switching device (col. 10, lines 33-46).

As to claim 12, Arimilli as modified above further teaches the buffer layer consists of at least one communication pathway switching device (col. 10, lines 33-46).

As to claim 23, Arimilli further teaches the processor comprises an interface for connection to other devices (Fig. 1B). However, Arimilli does not explicitly disclose the processor comprises a protocol layer; an information transfer layer to electronically transfer information on a physical medium between the protocol layer and the device; and a buffer layer to buffer an electronic transfer of information between the protocol layer and the information transfer layer. Walker teaches an information transfer layer (physical layer); a buffer layer (link layer); and a protocol layer (other upper layer(s) of the client/server to further process the data); wherein the information transfer layer is to electronically transfer information on a physical medium between the protocol layer and a device; the buffer layer is to buffer an electronic transfer of information between the protocol layer and the information transfer layer (Fig. 2 and col. 3, lines 49-67, and col. 4, lines 1-30). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include an information transfer layer, a buffer layer, and a protocol layer as taught by Walker in the system of Arimilli to expand communication to a network.

6. Claims 19-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Arimilli et al. (6,535,939) (hereinafter Arimilli) in view of Bales et al. (5,386,466) (herein after Bales).

As to claim 19, Arimilli teaches a processor, comprising: a routing agent (bus allocation unit and/or switch 401) to control one or more communication pathways in a processor (col. 6 lines 58-67, col. 7 lines 1-10); and an interface for connection to other devices (Fig. 1B). However, Arimilli does not explicitly disclose the processor comprises a protocol layer to process information and generate requests for information; an information transfer layer to transfer information on a physical medium between the protocol layer and a device; and a buffer layer to transfer information between the protocol layer and the information transfer layer. Bales teaches an information transfer layer (physical layer) to transfer information on a physical medium between a protocol layer and a device; a buffer layer (link layer) to transfer information between the protocol layer and the information transfer layer; and the protocol layer (other upper layer(s) to further process the data) is to process information and generate requests for information (Fig. 4 and Fig. 14). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include an information transfer layer, a buffer layer, and a protocol layer as taught by Bales in the system of Arimilli to expand communication to a network.

As to claim 20, Bales further teaches the information transfer layer consists of at least one communication pathway switching device (circuit switching of B channels is performed at the physical layer) and the buffer layer consists of at least one

communication pathway switching device (packet switching is performed at the link layer) (col. 24, lines 50-61).

As to claim 21, Arimilli further teaches the routing agent comprises a first component and a second component, the first component (part of the allocation unit) to set a bandwidth between the processor and the device (monitoring the bus usage on the system) (col. 10, lines 63-67), the second component (part of the allocation unit) to send a control signal to at least one communication pathway switching device (the switch system allocates the available configurable buses based on the change in workload and the priority of the components) (note col. 11, lines 1-11 and also col. 7, lines 1-10 wherein a mode bit may be used to tell the processor how the ports are configured).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, as the art discloses switch/routing agent between layers (Fig. 11):

US Pub. No 2002/0133620 Krause

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone numbers for the

organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Trisha U. Vu
Examiner
Art Unit 2189

uv
August 8, 2003

Glenn A. Auve
Primary Patent Examiner
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